Harshvardhan Singh

M.Tech, MVLSI
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ACADEMIC QUALIFICATIONS

Year	Degree/Certificate	Institute	CPI/%
2024 - Present	M.Tech (MVLSI)	Indian Institute of Technology, Kanpur	8.00/10
2020-24	B.Tech (EE)	Indian Institute of Technology, Jammu	8.15/10
2019	Class XII (CBSE)	Kendriya Vidyalaya, IIT Kanpur	81.4 %
2017	Class X (CBSE)	Kendriya Vidyalaya, IIT Kanpur	10/10

SCHOLASTIC ACHIEVEMENTS AND CERTIFICATIONS

- Secured **All India Rank 7733** in **JEE Advanced 2020** among **1,50,838** candidates.
- Secured **All India Rank 17164** in **JEE Mains 2020** among **10.23 lakh** candidates.
- Solved more than **450** questions on **Leetcode** and achieved a maximum **Codeforces** rating of **1454 (specialist)**.
- Solved more than **100** Verilog problems on **HDLBits**.
- Obtained an **A grade** in the VLSI system design course (EE619).

PUBLICATIONS

- **Harshvardhan Singh**, "Enhanced Liquid Adulteration Detection Using a Novel CSRR-Loaded Planar Microwave Probe", 2024 IEEE Microwaves, Antennas, and Propagation Conference **(MAPCON)**. DOI: 10.1109/MAPCON61407.2024.10923136

ACADEMIC PROJECTS

Academic Projects at IIT Kanpur:

- **Verilog Implementation of Backend module for an IC (Icarus Verilog)** (**EE619**)
  Mentor: Dr. Rik Dey, Dr. Chithra : Department of Electrical Engineering, IIT Kanpur
  - Designed a **mixed-signal IC backend** in Verilog with FSM, serial communication and moving average filtering.
- **Designed Logic Gates AOI21 and OAI21 using Static CMOS Logic with Layout (Cadence Virtuoso) (EE619)**
  Mentor: Dr. Rik Dey, Dr. Chithra : Department of Electrical Engineering, IIT Kanpur
  - Design, layout and characterization on Cadence Virtuoso and verified with DRC, LVS and PEX checks.
  - Characterized propagation delays for input transitions of 10 ps and 100 ps under output capacitances of 5 fF and 50 fF.
- **Design and Simulation of an 8-bit Dadda Multiplier in Verilog (Icarus Verilog)** (**Self Project**)
  - Implemented 8-bit unsigned multiplier in Verilog using behavioral half/full adders and verified with Icarus test bench.
- **Round Robin Arbiter Design using Verilog (Icarus Verilog)** (**Self Project**)
  - Developed a Verilog HDL arbiter for four requesters, implementing priority-based resource allocation.
- **Implementation of a Synchronous FIFO Memory Module using Verilog (Icarus Verilog)** (**Self Project**)
  - Developed an **8×16-bit** synchronous FIFO in Verilog with write/read/reset controls and full/empty status outputs.

M.TECH THESIS

Designing Wide-Band RF Power Amplifier (May'25 - Present)
Supervisor: Dr. Avinash Lahgere (EDCL, Department of Electrical Engineering, IIT Kanpur)

- Working on **Cadence AWR** to simulate RF matching networks; developed a novel matching network approach for PA design.

RELEVANT COURSES

• VLSI System Design (EE619) • Digital Design and Microcomputers (EED012U2M)	• Hardware Description Language Laboratory (EEP082U3G) • Analog VLSI circuits (EE610)	• Solid State Devices (EE614) • Analog Electronics (EEL016U3M)

TECHNICAL SKILLS

- **Languages: Verilog HDL**, C, **C++**.
- **Tools: Cadence Virtuoso**, Cadence AWR, Xilinx Vivado, LTspice, **Icarus Verilog**, MATLAB.

POSITIONS OF RESPONSIBILITY

- Class Representative for Electrical Engineering Batch at **IIT Jammu**. (*Nov'20-May'24*)
- Event Head, **Renao'23** (Annual Cultural Fest) at **IIT Jammu**. (*Jan'23-Mar'23*)

INTERESTS & HOBBIES

- **Hobbies :** Football, Swimming, Gym, Watching Movies, Driving.
- **Interests :** VLSI circuits, Spirituality, Astronomy and deep space exploration.